PATENT

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TITLE OF THE INVENTION

METHOD TO AVOID VIA POISONING IN DUAL DAMASCENE PROCESS

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method for making semiconductor devices.

Background of the Invention

[0002] The dual damascene process is widely used in semiconductor device fabrication. As part of fabricating the semiconductor device using the dual damascene fabrication process a conductive layer is formed on a substrate. Next, a barrier layer made from either silicon nitride or silicon carbide is deposited on the conductive layer to act as an etch stop. Shunt metal layers such as cobalt or tungsten may be used as a copper diffusion barrier.

[0003] The use of silicon nitride by itself as a barrier layer is undesirable due to its high dielectric constant (k).

[0004] The use of silicon carbide by itself as a barrier layer is also undesirable because silicon carbide has organic components and these organic components cause "via poisoning". As a result, these contaminants cause an undesirably high via resistance. Moreover, Silicon carbide is not a hermetic sealer, allowing undesirable moisture to diffuse through it causing undesirable effects in the semiconductor device.

BRIEF SUMMARY OF THE DRAWINGS

[0005] Examples of the present invention are illustrated in the accompanying drawings. The accompanying drawings, however, do not limit the scope of the present invention. Similar references in the drawings indicate similar elements.

[0006] Figures 1A-1F illustrate cross-sections during the formation of a semiconductor device using the dual damascene process according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0007] Described is a method to avoid via poisoning in a dual damascene process used during fabrication of a semiconductor device. The described method also reduces line-to-line capacitance in the interconnects of the semiconductor device. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known architectures, steps, and techniques have not been shown to avoid unnecessarily obscuring the present invention.

[0008] Parts of the description will be presented using terminology commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art.

[0009] **Figures 1A-1F** illustrate cross-sections during the formation of a semiconductor device using the dual damascene process according to one embodiment of the invention. As illustrated in Figure 1A a patterned conductive layer 101 is formed on dielectric material on substrate 100. Substrate 100 may be any surface, generated when making an integrated circuit, upon which a conductive layer may be formed. Substrate 100 thus may include, for example, active and passive devices that are formed on a silicon wafer such as transistors, capacitors, resistors, diffused junctions, gate electrodes, local interconnects, etc. Substrate 100 also may include insulating materials that separate such active and passive devices from the conductive layer or layers that are formed on top of them, and may include previously formed conductive layers.

[0010] Conductive layer 101 may be made from materials conventionally used to form conductive layers for semiconductor devices. In one embodiment, conductive layer

101 includes copper, and may be formed using a conventional copper damascene process. Although copper is preferred, other conducting materials including but not limited to metal alloys, aluminum, gold, and silver may be used instead. In one embodiment, conductive layer 101 may be planarized after it is deposited, using for example, chemical mechanical polishing ("CMP").

[0011] After forming a patterned conductive layer 101 on dielectric material on substrate 100, a first barrier layer 102A, comprising non-organic materials (e.g., silicon nitride), is formed on conductive layer 101. After forming the first barrier layer 102A, a second barrier layer 102B, comprising silicon carbide, is formed on first barrier layer 102A. Both barrier layers 102A and 102B serve to prevent an unacceptable amount of copper, or other metal, from diffusing into dielectric layer 103 of Figure 1B. In addition, barrier layer 102A also acts as an etch stop to prevent subsequent via etch steps from exposing conductive layer 101 to subsequent cleaning steps. Furthermore, first barrier layer 102A being comprised of non-organic materials, prevents organic contaminants from being deposited on the surface of conductive layer 101. Moreover, first barrier layer 102A prevents organic contaminants from other organic layers from being deposited on the surface of conductive layer 101.

[0012] Organic contaminants on the surface of conductive layer 101 is undesirable as the contact between conductive layer 101 and subsequent metal deposition on the surface of conductive layer 101 (e.g., metal deposition on the surface of conductive layer 101 in vias) may have a high interface resistance. The high interface resistance due to an electrically poor contact may cause the semiconductor device to fail. Moreover, the adhesion of silicon carbide (SiC) to copper (Cu) is not as good as the adhesion of silicon nitride (Si_3N_4) to copper.

[0013] First barrier layer 102A is preferably is made from silicon nitride. In one embodiment, first barrier layer 102A is less than 20 nanometers thick; preferably the thickness of first barrier layer 102A is between 1 nanometer and 7 nanometers.

[0014] As stated earlier, after forming the first barrier layer 102A a second barrier layer 102B is formed on first barrier layer 102A. As illustrated in Figure 1B, the second barrier layer 102B serves to further prevent an unacceptable amount of copper, or other metal, from diffusing into the dielectric layer 103 and serving as an etch stop layer. Silicon nitride comprising the first barrier layer 102A has a high k value and therefore a low k second barrier layer 102B is used to supplement the thickness of the first barrier layer, thereby acting as an etch stop layer and simultaneously maintaining an overall low value of k across the two barrier layers. The second barrier layer 102B is preferably made up of silicon carbide. In one embodiment, the thickness of the silicon carbide layer is less than 200 nanometers, preferably the thickness of the silicon carbide layer is between 10 nanometers and 200 nanometers, depending on the etch process selectivity.

[0015] Processes well known in the art e.g., a chemical vapor deposition process, a plasma enhanced chemical vapor deposition process, or even an atomic layer deposition process may be used to form barrier layers 102A and 102B. Barrier layers 102A and 102B should be thick enough to perform its copper diffusion inhibition and etch stop functions, but not so thick that it adversely impacts the overall dielectric characteristics resulting from the combination of barrier layers 102A and 102B and dielectric layer 103. Figure 1A illustrates a cross-section of the structure that results after conductive layer 101 and barrier layers 102A and 102B have been formed on substrate 100.

[0016] After the second barrier layer 102B is formed on the surface of the first barrier layer 102A, photoresist layer 130 may be patterned using conventional

photolithographic techniques, such as masking the layer of photoresist, exposing the masked layer to light, then developing the unexposed portions on the surface of the second barrier layer 102B. The resulting structure is shown in Figure 1B.

[0017] After photoresist layer 130 is patterned, via 107 as illustrated in Figure 1C is etched through dielectric layer 103, down to barrier layer 102B, followed by removing the photoresist generating the structure shown in Figure 1C. Conventional process steps for etching through a dielectric layer may be used to etch the via, e.g., a conventional anisotropic dry oxide etch process, or a conventional photoresist strip process. However, if a conventional photoresist strip process is used, a post ash clean may be needed to remove any residues after the photoresist strip process.

[0018] Another process for making a semiconductor device includes filling via 107 with a bottom anti reflective coating (BARC) e.g., a sacrificial light absorbing material (SLAM). The SLAM may comprise a dyed spin-on-polymer (SOP) or dyed spin-on-glass (SOG) that has dry etch properties similar to that of dielectric layer 103. The SLAM may be deposited by spin coating well known in the art. The type of SLAM used may depend upon the type of material used to form dielectric layer 103 e.g., if dielectric layer 103 is formed from silicon dioxide, using an SOG material to form the SLAM yields a better match between their respective etch rates. If dielectric layer 103 is formed from a polymer, then forming SLAM from an SOP material may produce a combination of materials having the desired selectivity. By filling via 107 with SLAM, substrate reflection that occurs during trench lithography--which could adversely affect dual damascene via and trench formation-- may be reduced or eliminated. Filling via 107 with SLAM may eliminate the need to use etch chemistry to etch the trench that is highly selective to dielectric layer 103 over barrier layer 102A, to ensure that the trench etch step will not etch through barrier layer 102A. After filling via 107 with SLAM,

the photoresist layer 130 may be patterened to define a trench formation region. In one embodiment, the etch chemistry chosen to etch the trench should remove the SLAM at about the same rate that it removes dielectric layer 103. Typically, SLAM is removed after the trench etch and ash process.

[0019] After etching via 107, via 107 and the surface of dielectric layer 103 may need further cleaning. In one embodiment, after forming via 107 a trench may be formed by patterning a second layer of photoresist 108 as illustrated in Figure 1D. Figure 1E illustrates the resultant structure showing a via and a trench after etching through a second portion of dielectric layer 103. After forming via 107 and trench 109, the formed via and trench may be cleaned by using a conventional cleaning chemicals, as is well understood by those skilled in the art. Although the process illustrates forming a via followed by forming a trench one skilled in the art will appreciate that a trench may be formed followed by forming the via.

[0020] After the via and the trench are formed, the portion of the barrier layers 102B and 102A that separates via 107 from conductive layer 101 may be removed to expose conductive layer 101 as shown in Figure 1F. In one embodiment, silicon carbide barrier layer 102B and silicon nitride barrier layer 102A are etched using a single etch pass. One skilled in the art will appreciate that the same gasses may be used to etch both the silicon carbide layer and the silicon nitride layer. In other embodiments, different gasses may be used to etch each barrier layer.

[0021] The process of the present invention provides a way to prevent via poisoning (i.e., prevents the contamination of vias due to the presence of organic materials) by using dual barrier layers comprising a layer of silicon carbide formed on a layer of silicon nitride.

[0022] Thus, a method has been disclosed to prevent via poisoning (i.e., prevents the contamination of vias due to the presence of organic materials) by using dual barrier layers comprising a layer of silicon carbide formed on a layer of silicon nitride. While there has been illustrated and described what are presently considered to be example embodiments of the present invention, it will be understood by those skilled in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the invention. Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.